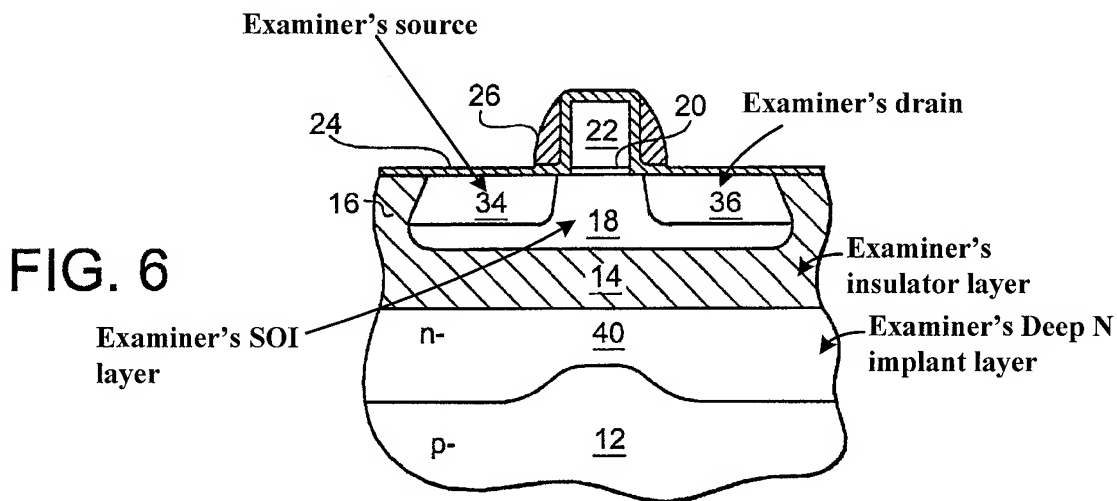


Remarks

For the reasons set forth below, Applicant respectfully submits that the claimed invention is allowable over the Krivokapic reference (U.S. Patent 6,339,244) as applied in the Final Office Action dated October 31, 2007.

Applicant reiterates and incorporates the arguments presented in the Response transmitted on December 26, 2007, and based thereon respectfully asserts that the Krivokapic reference does not disclose the claimed aspects directed to a Deep N implant layer formed between either the source or drain and an insulator layer. The Examiner improperly asserts that Krivokapic's n-silicon region 40 is formed between buried insulator layer 14 and source/drain junctions 34 and 36. As is clearly shown in Figure 6 of the Krivokapic reference (reproduced below), buried insulator layer 14 is located between n-silicon region 40 and source/drain junctions 34 and 36.



Thus, the cited portions of Krivokapic do not teach that layer 40 is formed between layer 14 and either source 34 or drain 36.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063 (or the undersigned).

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